IN THE CLAIMS:

The status of the claims is as follows. Any additional differences in the claims below and the current state of the claims are unintentional and in the nature of a typographical error.

1. (Previously Presented) A variable phase-shifting circuit comprising:

an input for receiving an input signal having a specified oscillation frequency;

an output for delivering an output signal having said specified oscillation frequency and having a variable phase-shift with respect to said input signal;

at least one control input for receiving a control signal which controls the phase-shift of said output signal with respect to said input signal; and

a synchronized oscillator comprising a synchronization input coupled to said input of the variable phase-shifting circuit and an output coupled to said output of the variable phase-shifting circuit, said synchronized oscillator having a variable free-running oscillation frequency controlled by said control signal;

wherein the input signal originates from a source that is external to the synchronized oscillator.

2. (Previously Presented) The circuit of Claim 1, wherein the synchronized oscillator further comprises an astable multivibrator circuit having a first branch and a second branch arranged in parallel between a positive supply terminal and a negative supply terminal or ground, and means for delivering into the first branch and into the second branch a respective quiescent current of a same specified value, said quiescent current being controlled by the control signal.

3. (Previously Presented) The circuit of Claim 2, wherein, for each branch, the means for delivering a quiescent current into the branch comprises a respective current source arranged in series in the branch, which delivers a current of a specified value, and wherein the control signal is a current control signal which is added to said current of a specified value.

4. (Withdrawn) Phase interpolator comprising:

- a signal output which delivers an output signal;

- at least one data input receiving a digital input value coded in P bits, where P is an integer, representing the difference between an actual instant of switching of a pulse of a signal to be interpolated and a desired instant of switching said output signal;

- N1 first variable phase-shifting circuits, where N1 is an integer strictly greater than one, each comprising an input which receives an input signal having the frequency of a reference signal, the input signals received by said respective inputs of said N1 variable phase-shifting circuits being respectively phase-shifted by 360°/N1, each variable phase-shifting circuit further comprising a control input receiving a control signal and an output which delivers an output signal corresponding to the signal received at the input phase-shifted based on said control signal, and each variable phase-shifting circuit comprising a synchronized oscillator having at least one synchronization input coupled to said variable phase-shifting circuit input , at least one output coupled to the said output of the variable phase-shifting circuit, said synchronized oscillator having a variable free-running oscillation frequency which is controlled by said control signal;

- a multiplexer having N1 inputs which receive the N1 signals delivered by the respective output of the N1 variable phase-shifting circuits and an output which delivers one of the said N1 signals based on the value of a given number Q of the most significant bits of the digital input value, where Q is an integer less than or equal to P.

5. (Withdrawn) The phase interpolator of Claim 4, further comprising a digital/analog converter having P-Q inputs which receive the P-Q least significant bits of the digital input value, and having an output which delivers, based on the value of said P-Q bits, an analog phase-shift correction signal which is delivered at the control input of at least one of the N1 first variable phase-shifting circuits.

6. (Withdrawn) The phase interpolator of Claim 4 wherein the phase-shift correction signal is delivered at the control input of each of the N1 first variable phase-shifting circuits.

7. (Withdrawn) The phase interpolator of Claim 4 further comprising a demultiplexer having an input receiving the phase-shift correction signal, at least N1 outputs respectively coupled to the control input of the N1 first variable phase-shifting circuits, and directing the phase-shift correction signal to the control input of one of the said N1 first variable phase-shifting circuits based on the value of the Q most significant bits of the digital input value.

8. (Withdrawn) The phase interpolator of Claim 4, further comprising a multiphase clock generator comprising:

- N1 second variable phase-shifting circuits identical to the N1 first variable phase-shifting circuits, connected in series via their respective inputs and outputs, the input of a first of said N1 second variable phase-shifting circuits receiving the reference signal;

- a phase comparator having a first input which receives the reference signal, a second input which is connected to the output of a last one of said N1 second variable phase-shifting circuits, and an output;

- a low-pass filter with an input coupled to the output of said phase comparator, and an output;

- an adaptation module having an input coupled to the output of said low-pass filter and at least N1 first outputs delivering N1 identical first calibration signals respectively, which are applied to the respective control inputs of said N1 second variable phase-shifting circuits.

9. (Withdrawn) The phase interpolator of Claim 8, wherein the adaptation module of the multiphase clock generator further comprises an N1 + 1-th output, delivering an N1 + 1-th calibration signal identical to the calibration signals generated by the N1 first outputs, and coupled to the digital-analog converter.

10. (Withdrawn) The phase interpolator of Claim 4 further comprising calibration means comprising:

- N2 third variable phase-shifting circuits identical to the N1 first variable phase-shifting circuits, connected in series via their respective inputs and outputs, the input of a first of said N2 third variable phase-shifting circuits receiving the reference signal;

- a phase comparator having a first input which receives the reference signal, a second input which is connected to the output of a last one of said N2 third variable phase-shifting circuits, and an output;

- a low-pass filter having an input coupled to the output of said phase comparator, and an output;

- an adaptation module having an input coupled to the output of said low-pass filter and at least N2 + 1 outputs delivering N2 + 1 identical second calibration signals respectively, among which N2 outputs are coupled to the respective control inputs of said N2 third variable phase-shifting circuits.

11. (Withdrawn) The phase interpolator of Claim 10, wherein the adaptation module of the calibration means includes N2 + 1 outputs delivering respectively N2 + 1 identical second calibration signals among which, in addition, the N2 + 1-th output is coupled to the digital-analog converter so as to provide it with a second reference value.

12. (Withdrawn) The phase interpolator of Claim 10, wherein the adaptation module of the calibration means includes N2 + 2xN1 outputs delivering respectively N2 + 2xN1 identical second calibration signals, among which, N1 other outputs are further coupled to the respective control inputs of the N1 second variable phase-shifting circuits of the multiphase clock generator, and among which N1 other outputs are coupled to the respective control inputs of the N1 first variable phase-shifting circuits.

13. (Withdrawn) The phase interpolator of Claim 4, wherein further comprising an input receiving a signal for activating/deactivating the multiplexer, to control the frequency of the output signal with respect to the reference signal frequency.

14. (Withdrawn) Digital frequency synthesizer comprising a phase accumulator and a phase interpolator coupled to said phase accumulator, wherein said phase interpolator comprises:

- a signal output which delivers an output signal;

- at least one data input receiving a digital input value coded in P bits, where P is an integer, representing the difference between an actual instant of switching of a pulse of a signal to be interpolated and a desired instant of switching said output signal;

- N1 first variable phase-shifting circuits, where N1 is an integer strictly greater than one, each comprising an input which receives an input signal having the frequency of a reference signal, the input signals received by said respective inputs of said N1 variable phase-shifting circuits being respectively phase-shifted by 360°/N1, each variable phase-shifting circuit further comprising a control input receiving a control signal and an output which delivers an output signal corresponding to the signal received at the input phase-shifted based on said control signal, and each variable phase-shifting circuit comprising a synchronized oscillator having at least one synchronization input coupled to said variable phase-shifting circuit input, at least one output coupled to the said output of the variable phase-shifting circuit, said synchronized oscillator having a variable free-running oscillation frequency which is controlled by said control signal;

- a multiplexer having N1 inputs which receive the N1 signals delivered by the respective output of the N1 variable phase-shifting circuits and an output which delivers one of the said N1 signals based on the value of a given number Q of the most significant bits of the digital input value,

where Q is an integer less than or equal to P.

15. (Withdrawn) The Digital frequency synthesizer of Claim 14, wherein the phase interpolator, further comprises a digital/analog converter having P-Q inputs which receive the P-Q least significant bits of the digital input value, and having an output which delivers, based on the value of said P-Q bits, an analog phase-shift correction signal which is delivered at the control input of at least one of the N1 first available phase-shifting circuits.

16. (Withdrawn) The Digital frequency synthesizer of Claim 14, wherein the phase-shift correction signal is delivered at the control input of each of the N1 first variable phase-shifting circuits.

17. (Withdrawn) The Digital frequency synthesizer of Claim 14, further comprising a demultiplexer having an input receiving the phase-shift correction signal, at least N1 outputs respectively coupled to the control input of the N1 first variable phase-shifting circuits, and directing the phase-shift correction signal to the control input of one of the said N1 first variable phase-shifting circuits based on the value of the Q most significant bits of the digital input value.

18. (Withdrawn) The Digital frequency synthesize of Claim 14, further comprising a multiphase clock generator comprising:

- N1 second variable phase-shifting circuits identical to the N1 first variable phase-shifting circuits, connected in series via their respective inputs and outputs, the input of a first of said N1 second variable phase-shifting circuits receiving the reference signal;

- a phase comparator having a first input which receives the reference signal, a second input which is connected to the output of a last one of said N1 second variable phase-shifting circuits; and an output;

- a low-pass filter with an input coupled to the output of said phase comparator, and an output;

- an adaptation module having an input coupled to the output of said low-pass filter and at least N1 first outputs delivering N1 identical first calibration signals respectively, which are applied to the respective control inputs of said N1 second variable phase-shifting circuits.

19. (Withdrawn) The Digital frequency synthesizer of Claim 18, wherein the adaptation module of the multiphase clock generator further comprises an N1 + 1-th output, delivering an N1 + 1-th calibration signal identical to the calibration signals generated by the N1 first outputs, and coupled to the digital-analog converter.

20. (Withdrawn) The Digital frequency synthesize of Claim 14 further comprising calibration means comprising:

- N2 third variable phase-shifting circuits identical to the N1 first variable phase-shifting circuits, connected in series via their respective inputs and outputs, the input of a first of said N2 third variable phase-shifting circuits receiving the reference signal;

- a phase comparator having a first input which receives the reference signal, a second input which is connected to the output of a last one of said N2 third variable phase-shifting circuits, and an output;

- a low-pass filter having an input coupled to the output of said phase comparator, and an output;

- an adaptation module having an input coupled to the output of said low-pass filter and at least N2 + 1 outputs delivering N2 + 1 identical second calibration signals respectively, among which N2 outputs are coupled to the respective control inputs of said N2 third variable phase-shifting circuits.

21. (Withdrawn) The Digital frequency synthesizer of Claim 20, wherein the adaptation module of the calibration means includes N2 + 1 outputs delivering respectively N2 + 1 identical second calibration signals among which, in addition, the N2 + 1-th output is coupled to the digital-analog converter so as to provide it with a second reference value.

22. (Withdrawn) The Digital frequency synthesizer of Claim 20, wherein the adaptation module of the calibration means includes N2 + 2xN1 outputs delivering respectively N2 + 2xN1 identical second calibration signals, among which, N1 other outputs are further coupled to the respective control inputs of the N1 second variable phase-shifting circuits of the multiphase clock generator, and among which N1 other outputs are coupled to the respective control inputs of the N1 first variable phase-shifting circuits.

23. (Withdrawn) The Digital frequency synthesizer of Claim 14, wherein further comprising an input receiving a signal for activating/deactivating the multiplexer, to control the frequency of the output signal with respect to the reference signal frequency.

24. (Previously Presented) A variable phase-shifting circuit comprising:

an input and an output having a specified oscillation frequency, said output having a variable phase-shift with respect to said input;

a control signal for controlling the phase-shift of said output with respect to said input; and

a synchronized oscillator having a synchronization input coupled to said input of said variable phase-shifting circuit and a second output coupled to said output of the variable phase-shifting circuit, said synchronized oscillator having a variable free-running oscillation frequency controlled by said control signal;

wherein the input of the variable phase-shifting circuit originates from a source that is external to the synchronized oscillator.

25. (Previously Presented) The circuit of Claim 24, wherein said synchronized oscillator further comprises an astable multivibrator circuit.

26. (Previously Presented) The circuit of Claim 25, wherein said astable multivibrator circuit further comprises a first branch and a second branch arranged in parallel between a positive supply terminal and a negative supply terminal or ground of the variable phase-shifting circuit.

27. (Previously Presented) The circuit of Claim 26 further comprising:

a delivery circuit arranged to deliver a respective quiescent current of a same specified value into said first branch and into said second branch.

28. (Previously Presented) The circuit of Claim 27, wherein said quiescent current is controlled by said control signal.

29. (Previously Presented) The circuit of Claim 27, wherein for each branch, said delivery circuit delivers said quiescent current into said branch.

30. (Previously Presented) The circuit of Claim 27, wherein each said branch comprising a respective current source arranged in series in the branch.

31. (Previously Presented) The circuit of Claim 30, wherein said respective current source delivers a current of a specified value.

32. (Previously Presented) The circuit of claim 31, wherein the control signal is a current control signal added to said current of a specified value.

33. (Previously Presented) A variable phase-shifting circuit comprising:

an input and an output having a specified oscillation frequency, said output having a variable phase-shift with respect to said input;

a control signal originating from a source external to said variable phase-shifting circuit to control the phase-shift of said output with respect to said input; and

a synchronized oscillator having a synchronization input coupled to said input of the variable phase-shifting circuit and a second output coupled to said output of the variable phase-shifting circuit, said synchronized oscillator having a variable free-running oscillation frequency controlled by said control signal; and

an astable multivibrator circuit having a first branch and a second branch arranged in parallel between a positive supply terminal and a negative supply terminal or ground of said variable phase-shifting circuit.

34. (Previously Presented) The circuit of Claim 33 further comprising:

a delivery circuit arranged to deliver a respective quiescent current of a same specified value into said first branch and into said second branch.

35. (Previously Presented) The circuit of Claim 34, wherein said quiescent current is controlled by said control signal.

36. (Previously Presented) The circuit of Claim 34, wherein for each branch, said delivery circuit delivers said quiescent current into said branch.

37. (Previously Presented) The circuit of Claim 34, wherein each said branch comprising a respective current source arranged in series in the branch.

38. (Previously Presented) The circuit of Claim 37, wherein said respective current source delivers a current of a specified value.

39. (Previously Presented) The circuit of claim 38, wherein the control signal is a current control signal added to said current of a specified value.